IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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M. Rudgers

In re Application of:

Farnworth et al.

Serial No.: 09/928,478

Filed: August 13, 2001

For: SEMICONDUCTOR DEVICE INCLUDING COMBED BOND PAD OPENING, ASSEMBLIES AND METHODS

Examiner: Unknown

Group Art Unit: 2841

Attorney Docket No.: 3401.5US (97-710.5)

CERTIFICATE OF MAILING

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PRELIMINARY AMENDMENT

Box Non-Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

IN THE SPECIFICATION:

Only paragraph **[0001]** in the Specification has been changed.

Clean version is presented below:

[0001] This application is a continuation of application Serial No. 09/651,460, filed August 30, 2000, now U.S. Patent 6,295,209 B1, issued September 25, 2001, which is a continuation of application Serial No. 09/464,992, filed December 16, 1999, now U.S. Patent 6,144,560, issued November 7, 2000, which is a continuation of application Serial No. 09/296,952, filed April 22, 1999, now U.S. Patent 6,091,606, issued July 18, 2000, which is a continuation of application Serial No. 09/002,063, filed December 31, 1997, now U.S. Patent 5,940,277, issued August 17, 1999.

IN THE CLAIMS:

Claims 4, 6, 13, 19 and 21 have been amended herein. All of the pending claims 1 through 21 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Also attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. A semiconductor device, comprising:

at least one contact pad positioned on a surface of the semiconductor device adjacent an edge thereof; and

a layer comprising dielectric material on at least a portion of said surface, said layer having a notch formed therein which exposes at least a portion of said at least one contact pad.

2. The semiconductor device of claim 1, wherein an edge portion of said layer adjacent said edge of the semiconductor device tapers from a surface of said layer toward said edge of the semiconductor device.

3. The semiconductor device of claim 2, wherein said edge portion of said layer comprises a bevel.

AD

4. (Amended) The semiconductor device of claim 1, wherein said notch is tapered from a surface of said layer toward said surface of the semiconductor device.

5. The semiconductor device of claim 1, wherein said layer covers substantially all of said surface.

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6. (Amended) The semiconductor device of claim 1, wherein said notch substantially surrounds said at least one contact pad.

7. The semiconductor device of claim 1, including a plurality of contact pads.

8. The semiconductor device of claim 7, wherein at least some of said contact pads are located adjacent said edge.

9. The semiconductor device of claim 8, wherein said layer includes regions extending laterally between adjacent contact pads of said at least some contact pads.

10. The semiconductor device of claim 1, wherein said dielectric material comprises a polymer.

11. The semiconductor device of claim 1, wherein said dielectric material comprises a photoimageable material.

12. A protective layer for a semiconductor device, comprising:
a substantially planar member comprising dielectric material; and
at least one notch formed adjacent an edge of said substantially planar member, said at least one notch being configured to expose at least a portion of a corresponding contact pad of the semiconductor device upon positioning the protective layer over a surface of the semiconductor device.

A4 13. (Amended) The protective layer of claim 12, further comprising a bevel along said edge.

14. The protective layer of claim 12, wherein at least one edge of said at least one notch is beveled.

15. The protective layer of claim 12, wherein said dielectric material comprises a polymer.

16. The protective layer of claim 12, wherein said dielectric material comprises a photoimageable material.

17. The protective layer of claim 12, including a plurality of notches located along said edge.

18. The protective layer of claim 12, wherein said substantially planar member is configured to substantially cover a surface of the semiconductor device upon assembly therewith.

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19. (Amended) The protective layer of claim 12, wherein said substantially planar member is configured to cover only a portion of a surface of the semiconductor device adjacent an edge thereof proximate to which at least one contact pad is located upon assembly of the protective layer with the semiconductor device.

20. The protective layer of claim 12, wherein said at least one notch is formed in said edge.

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21. (Amended) The protective layer of claim 12, wherein said at least one notch is configured to substantially surround the corresponding contact pad upon assembly of the protective layer with the semiconductor device.

REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth hereto prior to examination of the application on the merits.

Respectfully submitted,

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